H-3 DESIGN AND PERFORMANCE OF K-BAND POWER GAAS FETS ON MATCHED CARRIERS*

Leonard Rosenheck and Samuel Dow
Microwave Semiconductor Corporation
Somerset, New Jersey 08873

Carl Berglund and Mark Stevens
Massachusetts Institute of Technology
Lincoln Laboratory
Lexington, Massachusetts 02173

Abstract

Experimental relationships between the gain of K-band GaAs power FETs and the device geometries. Output powers as high as 1100mW with 4.3dB associated gain at 20.2 GHz have been measured. Matched carrier performance on both fused silica and sapphire is described.

Introduction

This paper discusses GaAs power FET devices and circuit development leading to matched amplifier modules at 100mW, 500mW, and 1000mW levels. The results of this work include output powers from a single chip as high as 1100mW with 4.3dB associated gain at 20.2 GHz, and 860mW with 5.8dB of gain and a power-added efficiency of 20.6% at 20.5 GHz.

Geometric considerations leading to high gain devices at K-band are described. The performance of devices having the same total gate periphery but with different gate widths and gate lengths are compared. In addition, some material parameters are related to RF performance. Finally, matched carriers are described which provide additional improvements in transistor performance.

Device Design

The K-band device design is based on work that had been reported earlier.[1] All the devices are fabricated utilizing a self-aligned gate process. This particular technique has been utilized to minimize channel length. Figure 1 is a cross-section of a channel that is less than 1.5μm wide. This technique minimizes the parasitic source resistance leading to improved gain at K-band frequencies.

Doping density variations were explored. The doping levels varied from $8x10^{16}$ atoms/cm^3 to $2.5x10^{16}$ atoms/cm^3. There is no obvious correlation of gain to the doping level. This suggests that doping is a non-critical parameter when related to RF gain at 20 GHz.

The gate length was varied from 0.5μm to 1.0μm. Although the data is scattered, as one would expect, the gain varies inversely with the gate length. Nearly 3dB of gain improvement was realized by decreasing the gate length from 1.0μm to 0.5μm. This improvement in gain can only be achieved, however, by minimizing any resulting increase in parasitic gate resistance.

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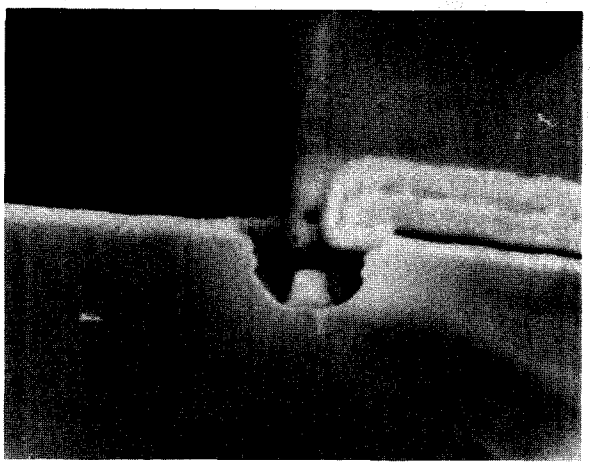

Fig. 1 Cross-sectional view of FET channel.

Devices designed specifically for K-band have individual gate widths which are either 50μm or 75μm. The gate widths were selected to minimize the total parasitic gate resistance. The trade-off between the gate width and gain was investigated by examining devices of 150μm and 100μm at K-band in addition to the above mentioned devices. Gain improvement in excess of 2dB by decreasing the gate width from 150μm to 50μm was observed.

The 500mW and 1000mW devices developed during the course of this work have peripheries of 75μm x 16 = 1.2mm and 75μm x 32 = 2.4mm respectively. A comparison between devices that were made with either periphery indicated that there is little, if any, degradation by directly scaling from 1.2mm to 2.4mm when devices are matched on carriers.

On-Carrier Matching

The 0.5W transistor performance reported previously included a typical 1.0dB operating bandwidth of 1.2 GHz.[2] This performance was achieved with the FET mounted on a carrier which includes alumina standoffs and leads for convenient connection to circuitry (CHIP-PAC mounting configuration) used in conjunction with microstrip impedance matching networks external to the FET package. In order to determine the limitations of this mounting configuration, this packaging arrangement was modified by replacing the active FET chip with a metallized chip to approximate a reference short-circuit termination, and the package impedance transformation was evaluated using a network analyzer. S-parameter measurements showed the reflection coefficient of the reference short to be displaced by 140° to

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150° from the package terminals at 20.5 GHz, with phase variation of ∿30° over the frequency band of 20 to 21 GHz. In addition, small but significant losses were also measured in the package.

In order to extend the operating bandwidth of these transistors, a low-loss packaging concept which minimizes parasitics was introduced. Carriers were designed and fabricated at Lincoln Laboratory which eliminate leads and standoffs, and place the microstrip impedance matching networks adjacent to the FET chip (Fig. 2). The carriers use .010" thick fused-silica or sapphire substrates soldered to a gold-plated invar base. The FET chip is flip-chip mounted on a pedestal at the center of the carrier and connected to the circuit by ribbons or wires. The chip is characterized using 50-ohm circuits to obtain S-parameters and large-signal parameters for designing matching networks.[3,4] The matching networks are comprised of distributed-element transmission-line sections to reduce fabrication complexity.

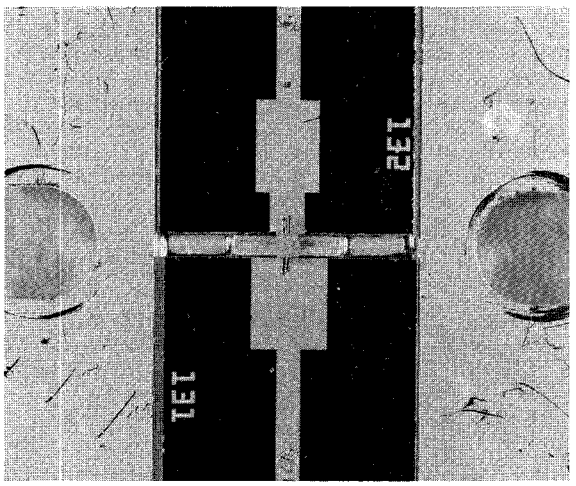


Fig. 2 MSC 100mW FET on Lincoln Laboratory Matched Carrier.

Matched Carrier Performance

The matched carriers have been utilized for the 100mW, 0.5W, and 1.0W transistors. The carrier base is identical for all transistors while appropriate matching circuitry is designed for each transistor size.

The typical performance for the 100mW transistor using fused-silica matching networks is shown in Fig. 3. Power output in excess of 160mW with over 5dB of gain and 30% power-added efficiency has been achieved. Typical small-signal gain is 6.5 to 7dB. The 1dB bandwidth was measured to be 3 GHz at a power input of 11.5dBmW (Fig. 4).

The matched carrier was also used for improving the bandwidth of the 0.5W transistors developed earlier.[1,2,3,4] A 1dB bandwidth of 1.8 GHz was achieved at a power input of +22 dBmW (Fig. 5). Power-added efficiency exceeding 25% has been achieved at 4.5dB of gain with over 440mW of output power. The typical small signal gain is 5.5 to 6.0dB (Fig. 6).

Figure 3.

TYPICAL PERFORMANCE OF MSC 100 mW FET

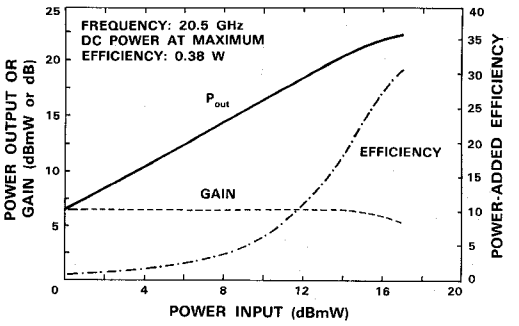


Figure 4.

FREQUENCY RESPONSE OF MSC 100 mW FET

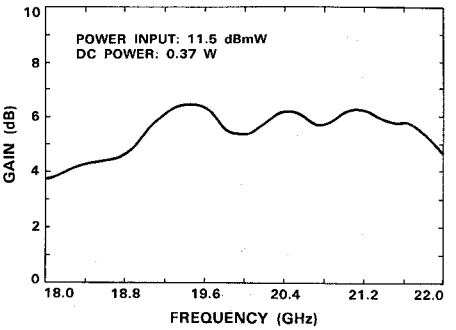


Figure 5.

FREQUENCY RESPONSE OF MSC 0.5 W FET

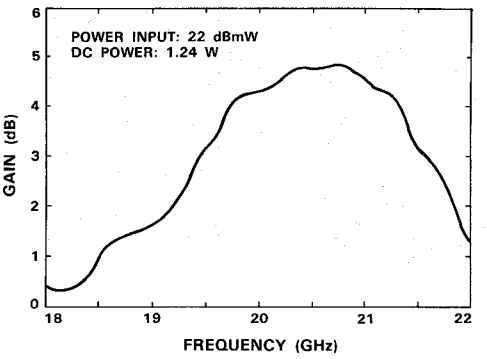
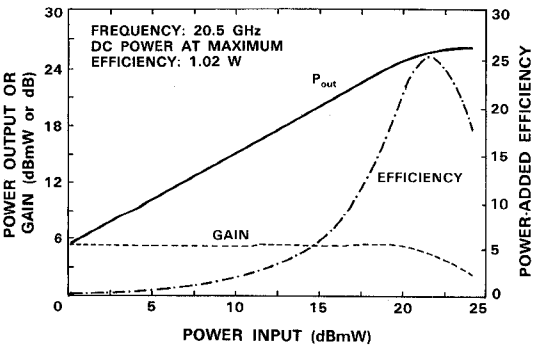


Figure 6.

TYPICAL PERFORMANCE OF MSC 0.5 W FET



Matching networks realized in both fused-silica and in sapphire have been utilized for the 0.5W FETs yielding similar performance.

Preliminary measurements were performed at Lincoln Laboratory on a 1.0W chip mounted in the CHIP-PAC configuration. Narrowband performance was achieved by matching the device input and output impedances with an air-dielectric slabline fixture. The best performance achieved with this device was 861mW of output power with 5.8dB of gain and 20.6% power-added efficiency at 20.5 GHz. Limitations of the input RF drive capability of the test setup prevented measurements at higher drive levels required to fully characterize this device. The small signal gain of the device was 7.2dB. Similar measurements performed at MSC have shown 1100mW of output power with 4.3dB of gain at 20.2 GHz.

Fig. 7 shows the MSC 1.0W FET chip mounted on a carrier with sapphire matching circuits. This device yielded the performance shown in Figs. 8 and 9. The 1dB bandwidth was measured to be ∿ 1 GHz with 860mW of output power and 3dB of gain. Power-added efficiency of greater than 20% was achieved, and the small signal gain exceeded 5dB.

Fig. 7 MSC 1.0W FET on Lincoln Laboratory Matched Carrier

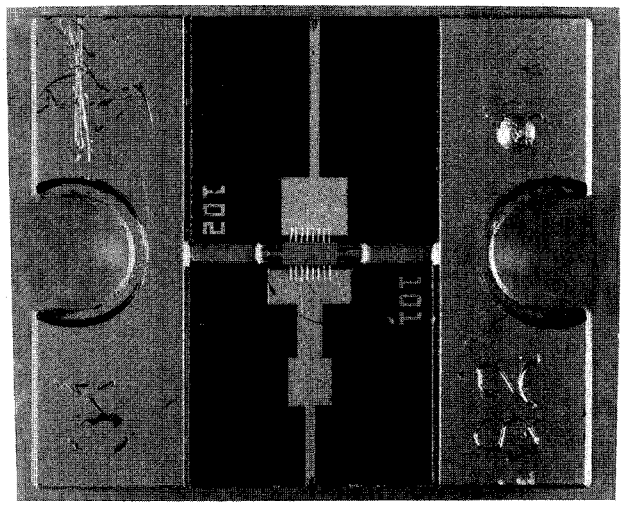


Fig. 8

PERFORMANCE OF 1.0 W FET ON MATCHED CARRIER

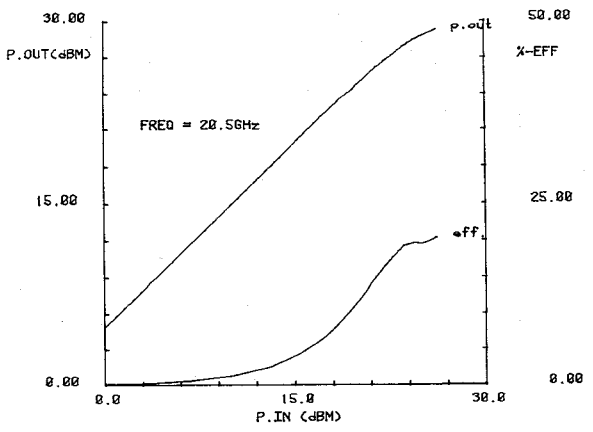
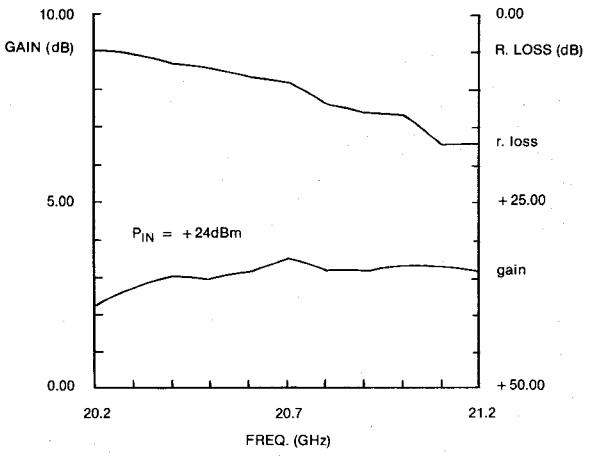


Fig. 9

FREQUENCY RESPONSE OF 1.0 W FET ON MATCHED CARRIER



Conclusion

High performance K-band GaAs MESFETs utilizing matched carriers have been produced. Transistor gain improvements have been realized through consideration of device geometry, device packaging, and matching circuit design. Power outputs of 0.16W, 0.5W, and .86W with corresponding power-added efficiencies of 30%, 25%, and 20% have been achieved for FETs mounted on matched carriers.

Acknowledgements

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